I Claim:

1. A method for passing a multiple bit wide data stream between a receiving device and a transmitting device on multiple data lines, the method of comprising:

producing a clock signal at the transmitting device and transmitting said clock signal to said receiving device on a clock line;

transmitting a predetermined synchronization pattern from said transmitting device to said receiving device on each of said multiple data lines to determine a sub interval clock phase for each data line that will successfully compensate for phase delays associated with said data lines and extract the synchronization pattern from each of said multiple data lines; and

extracting data from each of said multiple data lines at said sub interval clock phase determined for each of said multiple data lines to compensate for said phase delays.

2. The method of claim 1 further comprising determining a bit delay between a received data stream on one of said multiple data lines designated as a reference delay line and a received data stream on each of said multiple data lines not designated as said reference delay line and skew correcting the received data streams according to their respective bit delays such that said data streams are coherently transferred between said transmitting device and said receiving device.

3. The method of claim 1 wherein transmitting said clock signal on said clock line further comprises transmitting said clock signal on a differential set of clock lines, and wherein said multiple data lines further comprise multiple differential sets of data lines and wherein said data is transmitted in a bi-phase manner such that even bits are transmitted during high clock output states and odd bits are transmitted during low clock output states.

4. The method of claim 3 wherein determining a sub interval clock phase further comprises determining a first sub interval clock phase for a high clock output state half cycle and determining a second sub interval clock phase for a low clock output state half cycle and wherein sampling at said sub interval clock phase further comprises sampling at said first sub

interval clock phase during high clock output state half cycles and sampling at said second sub interval clock phase during low clock output state half cycles.

5. An interface for maintaining the coherency of data in N data streams being transmitted between a transmitting device and receiving device that includes a transmitting interface and a receiving interface, said interface comprising:

a sync pattern provider located on said transmitting device interface for providing a predetermined sync detect pattern;

a clock generator for generating a clock signal;

a sync multiplexer located at said transmitting interface for receiving said N data streams from said transmitting device and said sync detect pattern from said sync pattern provider and selectively multiplexing said sync detect pattern and said N data streams onto N+1 data lines;

a test line controller designating one of said N+1 data lines as a sync detect line and designating N of said N+1 data lines as data transmitting lines so that said sync multiplexer transmits said sync detect pattern to said receiving interface on a selected sync detect line, and wherein said sync multiplexer transmits said N data streams to said receiving interface on each one of said N+1 data lines not selected as said sync detect line;

a clock receiving circuit positioned at said receiving interface for receiving said clock;

N+1 samplers positioned at said receiving device interface for receiving and sampling said N data streams and said sync detect pattern on said N+1 data lines and providing said data streams to said receiving interface wherein said samplers sample said sync detect pattern at multiple phase time delays to produce multiple phase test patterns;

comparators for comparing each one of said multiple phase test patterns to said phase sync detect pattern to determine if any of said multiple phase test patterns are equivalent to said phase sync detect pattern and designating such equivalent phase test patterns as selected phase test patterns;

storage devices for storing a phase time delay corresponding to the phase time delay of one of said selected phase test patterns;

wherein during a predetermined number of clock cycles said sync multiplexer cycles said sync detect line through each one of said N+1 data lines such that an associated phase time delay is determined and stored for each of said N+1 data lines and wherein said samplers sample each of said N data streams based upon said associated phase time.

6. The interface of claim 5 further comprising:

said sync pattern provider providing a predetermined sync detect pattern having a first phase sync detect pattern and a second phase sync detect pattern;

said clock generator generating a clock signal having a first clock phase period and a second clock phase period at said transmitting device;

said N+1 samplers sampling said sync detect pattern at multiple first phase time delays during said first clock phase to produce multiple first phase test patterns and sampling said sync detect pattern at multiple second phase time delays during said second clock phase to produce multiple second phase test patterns;

said comparators comprising:

comparators for comparing each one of said multiple first phase test patterns to said first phase sync detect pattern to determine if any of said multiple first phase test patterns are equivalent to said first phase sync detect pattern and designating such equivalent first phase test patterns as selected first phase test patterns; and

the same comparators for comparing each one of said multiple second phase test patterns to said second phase sync detect pattern to determine if any of said multiple second phase test patterns are equivalent to said second phase sync detect pattern and designating such equivalent second phase test patterns as selected second phase test patterns;

said storage devices storing first and second phase time delays corresponding respectively to the phase time delays of one of said selected first and second phase test patterns;

during a predetermined number of clock cycles, said sync multiplexer cycling said sync detect line through each one of said N+1 data lines such that an associated first phase

time delay and an associated second phase time delay are determined and stored for each of said N+1 data lines and wherein said samplers extract data from each of said N data streams based upon said associated first phase time delay during said first clock phase and based upon said associated second phase time delay during said second clock phase.

7. The interface of claim 6 wherein said comparators further comprise controllers for selecting one equivalent first phase test pattern as an optimal selected first phase test pattern based upon predetermined criteria when more than one of said multiple first phase test patterns are equivalent to said first phase sync detect pattern and wherein said comparators further comprise controllers for selecting one equivalent second phase test pattern as an optimal selected second phase test pattern based upon predetermined criteria when more than one of said multiple second phase test patterns are equivalent to said second phase sync detect pattern.

8. The interface of claim 5 wherein said sync pattern provider further comprises an M bit serial shift register that serially provides an M bit sync detect pattern to said sync multiplexer in response to said clock signal.

9. The interface of claim 6 wherein said storage devices further comprise N+1 sets of M shift registers wherein M is equal to a number of bits in said first phase sync detect pattern plus a number of bits in said second phase sync detect pattern and wherein said sets of M shift registers serially receive said first phase sync detect pattern and said second phase sync detect pattern from said N+1 data lines.

10. The interface of claim 5 wherein said N+1 samplers further comprise clock buffers positioned between said clock line and N+1 sampling devices such that said sampling devices sample the N data streams at the associated first and second phase time delays for the respective data lines.

11. The interface of claim 6 wherein said comparators further comprise comparing storage registers for storing said multiple sampled first phase test patterns and said multiple

sampled second phase test patterns and comparators for comparing said stored multiple first and second phase test patterns to said predetermined first and second phase sync detect patterns to determine if any of said multiple first phase test patterns are equivalent to said first phase sync detect pattern and designating such equivalent first phase test patterns as selected first phase test patterns and to determine if any of said multiple second phase test patterns are equivalent to said second phase sync detect pattern and designating such equivalent second phase test patterns as selected second phase test patterns.

12. The interface of claim 5 further comprising an order multiplexer for separating said sync detect pattern from said data streams and providing said data streams to said receiving device.

13. The interface of claim 5 further comprising bit delay detecting and correcting devices, said bit delay detecting and correcting devices comprising:

a counter for determining a number of clock cycles that pass between reception of the sync detect pattern on a data line designated a reference data line and reception of the sync detect pattern on a next data line designated as the sync test line;

a skew detector for comparing a predetermined number of clock cycles that pass between transmission of the sync detect pattern on the reference data line and transmission of the sync detect pattern on the next data line to the determined number of clock cycles between reception of the sync detect pattern on the reference data line and the next data line designated as the sync test line to determine a data skew between the reference data line and the data line designated as the sync test line wherein said skew detector determines a data skew for each data line with respect to said reference data line; and

a bit delay compensator for skew correcting data received on each of said N+1 data lines by said data skew between said respective lines of said N+1 data lines to produce skew corrected data and providing said skew corrected data to said receiving device.

14. A method for maintaining the coherency of bi-phase data being transmitted in parallel between a transmitting device and a receiving device said data comprising sets of data bits being transmitted in N data streams on N+1 data lines, a sync line and a clock line, said method comprising:

generating a sync signal including a predetermined first half sync detect pattern and a predetermined second half sync detect pattern at said transmitting device;

producing a bi-phase clock signal including a first phase clock period and a second phase clock period at said transmitting device;

transmitting said bi-phase clock signal between said transmitting device and said receiving device;

designating one of said N+1 data lines as a sync test line;

transmitting said sync signal including said first half sync detect pattern and said second half sync detect pattern to said receiving device on said sync test line;

transmitting said each of said N data streams to said receiving device on a one of said N+1 data lines;

sampling said received sync signal at multiple sampling times to produce multiple first phase and second phase test data sets;

comparing said multiple test data sets to said first half sync detect pattern to determine which of said multiple test data sets sampled during said clock period corresponds to said first half sync detect pattern;

storing a phase time delay that corresponds to one of said multiple test data sets that corresponds to said first half sync detect pattern;

comparing said multiple test data sets to said second half sync detect pattern for each of said multiple data sets to determine which of said multiple test data sets sampled during said clock period corresponds to said second half sync detect pattern;

storing a second phase time delay that corresponds to one of said multiple test data sets that corresponds to said second half sync detect pattern;

sampling future data streams received on said data line designated as said sync test line at sampling times based on said stored first and second phase time delays; and

cycling through said N+1 data lines by designating a new one of said N+1 data lines as said sync test line after a predetermined number of clock cycles and calculating associated first and second phase time delays respectively for first phase clock periods and second phase clock periods for each of said N+1 data lines and sampling future data streams on each of said N+1 data lines at sampling times based on said associated first and second phase delays during each said clock period.

15. The method of claim 14 further comprising indicating a lock condition if a first phase test data set that is equivalent to said first half sync detect phase and a second phase test data set that is equivalent to said second half sync detect pattern is located for each of said N+1 data lines for two consecutive cycles of the sync test line though said N+1 data lines.

16. The method of claim 14 further comprising indicating an unlock condition if a first phase test data set that is equivalent to said first half sync detect pattern and a second phase test data set that is equivalent to said second half sync detect pattern are not located for all of said N+1 data lines during any consecutive cycling of the sync test line through said N+1 data lines.

17. The method of claim 14 wherein sampling said received sync signal during said first phase clock period and said second phase clock period at multiple sampling times to produce multiple first phase and second phase test data sets further comprises sampling said received sync signal at a higher rate than a data rate of said data streams such that all of said multiple first phase and second phase test data sets are produced in the time required to transmit said first and second half sync detect patterns.

18. The method of claim 14 wherein a predetermined number of clock cycles pass between transmission of the sync detect pattern on a data line designated as the sync test line and transmission of the sync detect pattern on a next data line designated as the sync test line, said method further comprising:

designating a data line designated as the sync test line as a data skew reference line;

counting the number of clock cycles between reception of said sync detect pattern on said data skew reference line and reception of said sync detect pattern on a next data line designated as the sync test line;

comparing the counted number of clock cycles between reception of the sync detect pattern on the data skew reference line and the data line designated as the next sync test line to a predetermined number of clock cycles between transmission of the sync detect pattern on said data skew reference line and said data line designated as the next sync test line to determine a data skew value of said data line with respect to said data skew reference line;

determining a data skew value for each of said N+1 data lines with respect to said data skew reference line; and

correcting for data skew between said data streams by time shifting said data streams with respect to said data stream on said data skew reference line based upon said data skew values.